IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): John M. Cohn, et al.

Examiner: John P. Trimmings

Serial No: 10/709,754

Art Unit: 2117

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Docket: BUR920040001US1 (17382)

For: A SYSTEM AND METHOD OF PROVIDING ERROR DETECTION AND CORRECTION CAPABILITY IN AN INTEGRATED CIRCUIT USING REDUNDANT LOGIC CELLS OF AN EMBEDDED FPGA

Dated: August 9, 2007

Confirmation No: 3753

Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, Virginia 22313-1450

RESPONSE UNDER 37 C.F.R. §§1.111 AND 1.143

Sir:

In response to the Office Action dated July 9, 2007, applicants provisionally elect, without traverse, the subject matter of Group I, i.e., Claims 1-20 and 28-30, for continued prosecution in the above-identified patent application.

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being deposited with the United States Patent & Trademark Office via Electronic Filing through the United States Patent and Trademark Office e-business website, on the date shown below.

Dated: August 9, 2007

Steven Fischman